

## REMARKS

Claims 1-17 are pending in the application. Claims 1, 6, 9, 11, and 15 are the independent claims. Claims 1, 6, 9 and 11 have been amended to more clearly set forth the metes and bounds of patent protection desired. Claims 16 and 17 are new. Because none of the cited references disclose separately or in combination a *plurality of parallel texture pipelines*, the Applicants respectfully submit that the pending claims are patentable over the cited references and should be allowed.

### **The Claims Patentably Define The Invention Over *Migdal* in view of *Duluk*.**

Claims 1, 4 and 6-9 have been rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,392,655 to Migdal, et al. (“Migdal”) in view of U.S. Patent No. 6,525,737 to Duluk, Jr. (“Duluk”). The Applicants respectfully traverse this rejection because the cited references do not separately or in combination teach or suggest all the features of the recited claims.

Claim 1 has been amended to recite a “plurality of sets of parallel texture pipeline state variable queues.” *Migdal* fails to teach or suggest these features. Instead, *Migdal* describes a method of using a fine grain multi-pass technique to enhance the performance of a single texture pipeline. *See, e.g.*, Abstract; Figs. 1-3, 5; and col. 4:59-61 (“Only one texture processing hardware unit is used. Multiple dedicated texture processing hardware units are not necessary.”).

Like *Migdal*, *Duluk* only discloses a graphics processor having a single pipeline. *See, e.g.*, Fig. 5A (showing a single “TEX” texture processing block); *see also* col. 6:38-44 (discussing a single texture block). Nothing in *Duluk* teaches or suggests the use of parallel texture pipelines or parallel texture pipeline state variable queues, as recited by claim 1. Accordingly, claim 1 is patentable over *Migdal* in view of *Duluk* and should be allowed. Claims 4, and 6-9 recite similar subject matter and are therefore patentable for the same reasons as claim 1.

### **The Claims Patentably Define The Invention Over *Migdal* in view of *Duluk* and *Fliflet*.**

Claims 2-3 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Migdal* in view of *Duluk* and U.S. Patent App. No. US2002/0140710 to Fliflet (“Fliflet”). The Applicants respectfully traverse this rejection. Nothing in *Fliflet* makes up for the deficiencies of

*Migdal* or *Duluk*. *Fliflet* merely describes a method for optimizing graphics performance by balancing graphics software and hardware workloads. *Fliflet* fails entirely to teach or suggest parallel texture pipelines. Thus, claims 2 and 3, which depend from claim 1, are patentable over *Migdal* in view of *Duluk* and *Fliflet* and should be allowed.

**The Claims Patentably Define The Invention Over *Migdal* in view of *Duluk* and *Melo*.**

Claims 5 and 10 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Migdal* in view of *Duluk* and U.S. Patent No. 6,243,817 to Melo, et al. (“*Melo*”). The Applicants respectfully traverse this rejection as well because *Melo* fails to teach or suggest parallel texture pipelines. *Melo* merely describes a method of dynamically reducing power consumption within input buffers of a bus interface unit. Thus, claims 5 and 10, which depend from claims 1 and 9, respectively, are patentable over *Migdal* in view of *Duluk* and *Melo* and should be allowed.

**The Claims Patentably Define The Invention Over *Migdal* in view of *Duluk* and *Battle*.**

Claims 11-15 have been rejected under 35 U.S.C. §103(a) as being unpatentable over *Migdal* in view of *Duluk* and U.S. Patent No. 6,462,743 to Battle, et al. (“*Battle*”). The Applicants respectfully traverse. As noted, *Migdal* and *Duluk* fail to show multiple parallel texture pipelines. *Battle* fails to show this subject matter as well. *Battle* merely describes a method of improving the efficiency of a graphics pipeline by converting graphics commands to component elements that include state information and mode parameters. *Battle* fails entirely to teach or suggest parallel texture pipelines. Thus, claims 11-15 are patentable over *Migdal* in view of *Duluk* and *Battle* and should be allowed.

**The New Claims Patentably Define The Invention of the Cited References.**

Newly added claims 16 and 17 recite a method of synchronizing texture processors, comprising “accumulating polygon state variables in accumulation portions of a plurality of state variable queues, each of said state variable queues associated with a respective parallel texture pipeline processor.” None of the cited references teaches or suggests this combination of features. Thus, Applicants respectfully submit that claims 16 and 17 are patentable and should be allowed.

## Conclusion

In view of the above amendments and remarks, the Applicants respectfully submit that the present application is now in condition for allowance. A timely Notice to that effect is earnestly solicited. The Examiner is invited to contact the undersigned at (202) 220-4200 to discuss any aspect of the application.

Respectfully submitted,

KENYON & KENYON

Date:

July 30, 2002

By:

Clyde E. Findley (Reg. No. 50,724)  
(Attorneys for Intel Corporation)

KENYON & KENYON  
1500 K Street, NW  
Washington, DC 20005  
Phone: (202) 220-4200

462076\_1.DOC